What is claim d is:

1. A wiring substrate comprising:

a base made of a metal; and

at least one layer wiring formed on the base through an insulating film, the layer wiring having a wiring film formed by electroplating,

wherein the base is selectively etched.

2. A method for fabricating a wiring substrate comprising the steps of:

forming at least one layer wiring on a base made of a metal through an insulating film, the layer wiring having a wiring film formed by electroplating; and

selectively etching the base.

3. A wiring substrate comprising:

a base made of a metal;

a first insulating film having openings formed on the base;

at least one layer wiring formed on the first insulating film, the layer wiring having a wiring film made of a metallized film at a lower portion; and

a second insulating film formed on a region that the layer wiring is formed, except for a portion,

wherein the base is selectively etched to partially expose a back surface of the wiring film.

4. The wiring substrate according to claim 3 wherein the base is partially r moved to form at least one select d from a group having a ground layer, a power source plane, a

terminal, a dam and a reinforcement portion, and the opening formed in th first insulating film is filled with th wiring film to connect the wiring film to at least one selected form the group.

5. The wiring substrate according to claim 3 wherein the metallized film is made of a wiring film material and a material having selective etching property.

6. The wiring substrate according to claim 3 wherein the partially removed base forms a terminal for connecting with other member.

7. The wiring substrate according to claim 3 wherein a terminal is formed on a portion of the region that the layer wiring is formed, by partially removing the second insulating film, and a hole for filling a buffer is formed at a position corresponding to the terminal of the base, the buffer is filled in the hole.

8. The wiring substrate according to claim 3 wherein on the region that the layer wiring is formed, a portion where the second insulating film is partially removed serve as an opening for forming a bump electrode at which the layer wiring is partially exposed, and the bump electrode to be connected to the LSI chip by flip chip bonding are formed in the opening.

9. The wiring substrate according to claim 3 wherein on the region that the layer wiring is formed, a portion where the second insulating film is partially removed serve as an opening for forming a bump electrod at which the lay r wiring is partially exposed, and the bump el ctrode to be connected

to oth r member are formed in the op ning.

10. A wiring substrate comprising:

at least one layer wiring film formed on one side of the resin film having openings; and

two kinds of metal bumps which are formed on the other side of the resin film, which are connected to the layer wiring film through the openings and which are different in height from each other.

11. The wiring substrate according to claim 10 wherein lower metal bumps are bumps for flip chip bonding, and an LSI chip is bonded to the lower metal bumps.

12. The wiring substrate according to claim 10 wherein an LSI chip is disposed on the one side of the resin film where the layer wiring films are formed.

13. A method for fabricating a wiring substrate comprising the steps of:

selectively forming first solder films on one main surface of a base metal;

forming a metal film on the one main surface of the base metal including the first solder films;

forming an insulating film having openings on the metal film at positions corresponding to metal bumps to be formed later;

forming at least one layer wiring on the insulating film;

forming second solder films on the other main surface of the base metal at positions wher higher m tal bumps ar to

be formed; and

etching the base metal from the other main surfac sid using the second solder films as masks, and tching the metal film using as masks the first solder films and the second solder films, thereby forming higher metal bumps made from the metal film and the base metal and lower metal bumps made from the metal film.

14. The method according to claim 13 wherein reflowing treatment is applied to the first and second solder films after forming the higher metal bumps and the lower metal bumps, so that the higher metal bumps and the lower metal bumps are covered with solders of the first and second solder films.

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